HOT-SWAP PROTECTION CIRCUIT

APPENDIX A

IXYS

IXHQ 100PI
IXHQ 100SI

Negative Voltage Hot Swap Controller with Active Power Filter

Features

- **Live Insertion and Removal Power Manager**
- **Adjustable Power-on slew rate**
- **Autodetect of Load Open Circuit or -VIN Disconnection**
- **Controlled Time-Delay**
- **Operates from –9 V to External MOSFET Voltage Limit**
- **Fault Indication Output (microprocessor reset).**
- **Board Insertion/Removal Detector Input**
- **Protection During Turn-On**
- **Low frequency Power Active Filter**
- **Adjustable Electronic Circuit Breaker**
- **V_{in} undervoltage with GSNSin input**

Applications

- **Arcless card insertion and removal**
- **Central Office Switching Hardware**
- **Circuit Boards From -48 V Distributed Power Supplies**
- **Circuit Board Power Manager and Noise Filter**
- **Circuit Board Hot Swap Protector and Manager**
- **Electronic Circuit Breaker**
- **Wireless Local Loop Antennas**
- **Cable TV Antenna**

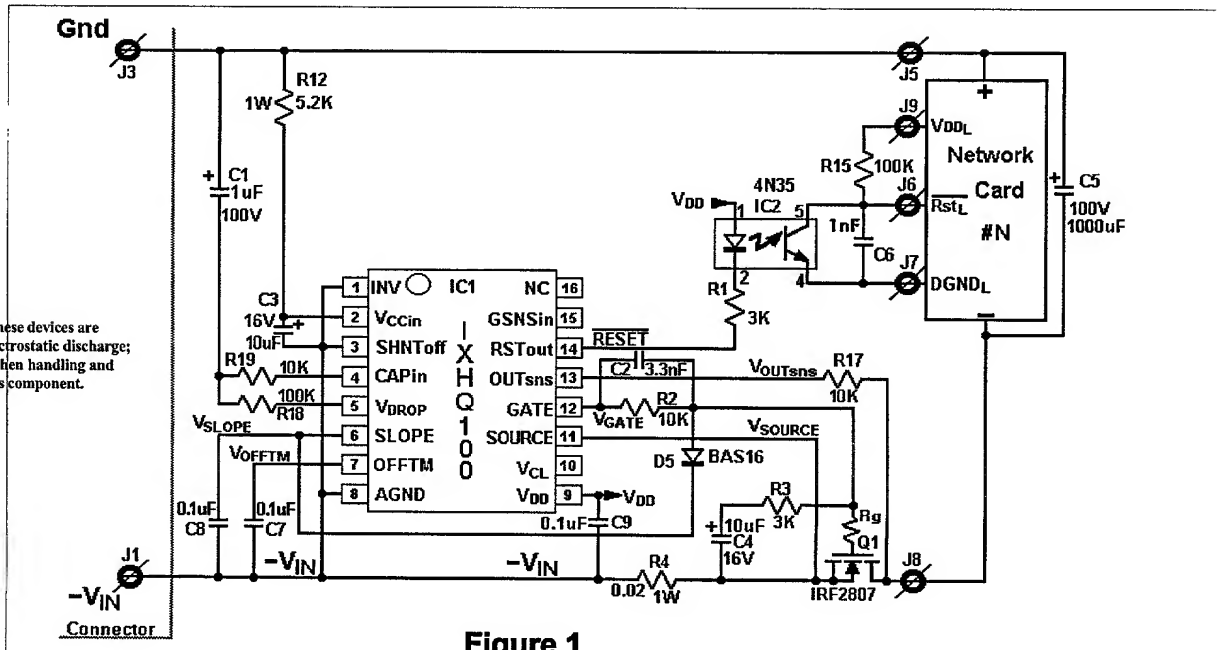
Description

The IXHQ100 is a live insertion and removal hot swap controller with a built-in power noise filter. It incorporates all the active circuitry necessary to protect circuit boards during live insertion or removal (insertion or removal when the system power is active). Additionally, the IXHQ100 incorporates two unique features: power active filter for powerline noise suppression and power auto-disconnect detector which eliminates the need of additional staggered pins.

The IXHQ100 shunt regulator ensures a wide operating voltage range (with the external MOSFET breakdown voltage as limit). The active power filter reduces power source output impedance, producing "clean" load power. The IXHQ100 allows continuous load current rise adjustments, presettable maximum current limits, and user selectable fault indication turn off times for resetting µPs and other synchronous board level systems. For added flexibility, GSNSin pin is available to implement either circuit board insertion/removal detection or ground detection.

US Patents Pending.

Typical Application with Auto-Disconnect Detector



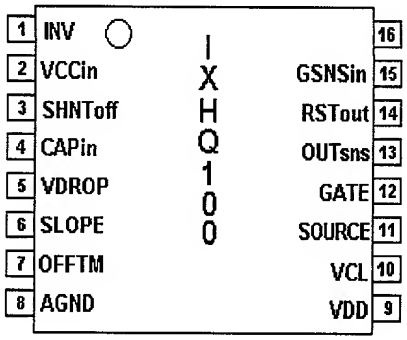
CAUTION: These devices are sensitvie to electrostatic discharge; take caution when handling and assembling this component.

Figure 1

Absolute Maximum Ratings

Symbol	Definition	Max. Rating
V_{CC}-V_{AGND}	Voltage applied V_{CCin} to AGND	Shunt Off: -0.3 V to 16 V
	Shunt On:	-0.3 V to 14 V
	Shunt On for 10 seconds	14V to 16 V
	All other pins except V_{DC}	-0.3 V to V_{CCin} + 0.3 V
I_{VDD}	V_{DD} Load Current	60 mA
T_{JM}	Maximum Junction Temperature	125 °C
T_{J0}	Operating Temperature Range	-40 °C to 85 °C
T_{stg}	Storage Temperature Range	-40 °C to 150 °C
I_{DD}	Supply Current with Shunt On	25 mA

Pin Description



Electrical Characteristics

Unless otherwise noted, T_A = 25 °C; $-V_{IN}$ = 48 V, AGND connected to $-V_{IN}$, $V_{SHUNToff}$ = 5 V, V_{CC} = 12 V, V_{GSNSin} = 12 V. All voltage measurements with respect to AGND. IXHQ100 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Supply current	V_{CC}=12 V, $V_{SHUNToff}$ = V_{CC}, all outputs unloaded.		2	3	mA
$V_{CCSHUNT}$	V_{CC} shunt regulation voltage	I_{CC} forced to 10 mA when shunt is off	12	13.8	16	V
$V_{THSHUNToff}$	SHUNToff input threshold voltage	V_{CC} = 15 V, monitor RST_{OUT}	1	1.5	2	V
$I_{SHUNToff}$	SHUNToff input bias current		-1	0	1	µA
V_{THINV}	INV input threshold voltage	V_{CC} = 12 V, monitor RST_{OUT}	6	8	10	V
R_{INV}	INV input resistance		70	130	180	KΩ
V_{THGSNS}	GSNS sense input threshold voltage	V_{CC} = 12 V, monitor RST_{OUT}	4.5	5.8	6	V
I_{GSNSin}	GSNSin input bias current		-2.6	-2.3	-2	µA
I_{CAPin}	CAPin input bias current		-1	0	1	µA
V_{VDROP}	Active filter offset voltage		0.7	0.9	1.1	V
R_{VDROP}	V_{DROP} input resistance		50	70	90	KΩ
I_{SLOPE}	SLOPE capacitor charging current	V_{OFFTM} = 5 V, $V_{GSOURCE}$ = 0 V V_{CAPin} = 5 V	70	85	110	mA
$R_{SLOPEDCHG}$	SLOPE capacitor discharge resistance	V_{DROP} = 5 V, IVT = V_{CC} V_{SOURCE} = 0 V, V_{CAPin} = 5 V		90	200	Ω
I_{OFFTM}	OFFTM capacitor charging current	V_{DROP} = 5 V, V_{SOURCE} = 0 V V_{CAPin} = 5 V	80	100	120	mA
$R_{OFFTMCHG}$	OFFTM capacitor discharge resistance			111	200	Ω
$V_{THOFFTM}$	OFFTM input threshold voltage	OFFTM input voltage when SLOPE input voltage starts its ramp	3.8	4.5	5.5	V
V_{CL}	Overcurrent threshold bias voltage		90	125	150	mV

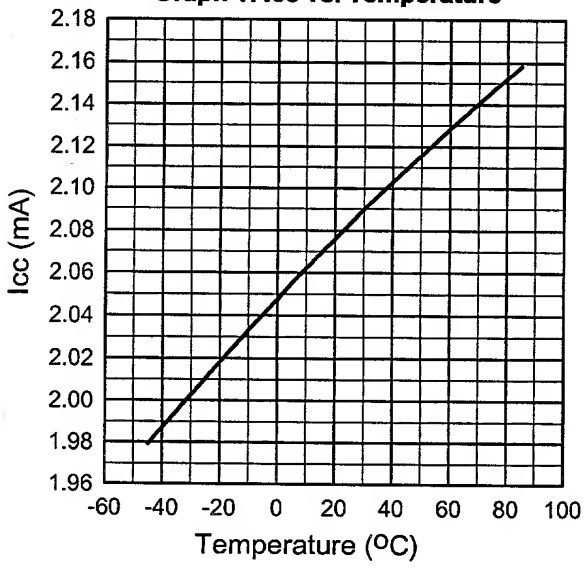
Electrical Characteristics (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
R_{VCL}	VCL bias resistance		4	6	10	kΩ
t_{OC}	Overcurrent detection to GATE output delay	V_{CAPin} = 0 V; V_{OUTsns} = 5 V V_{SOURCE} input is a step at t = 0s from 0 V to 200 mV		20	30	ms
dv_{GATE}/dt	GATE output slew rate	C_{SLOPE}= 100 nF	0.5	0.8	1.1	V/ms
V_{GATE}	Maximum GATE output voltage	V_{CAPin} = 0 V; R_{load} = 10 KΩ V_{OUTsns} = 5 V		13.8	15	V
I_{GATE}	GATE pull-up current	Gate drive on, V_{GATE} = 0 V		-15	-10	mA
I_{GATE}	GATE pull-down current	Gate drive off V_{GATE} = 10 V	10	20		mA
V_{DD}	V_{DD} regulator output Voltage	3.3K Resistive load between V_{DD} output and AGND	5	5.75	6.5	V
I_{RSTout}	RSTout drive current	Force V_{RSTout} =1 V during fault condition	2.4	3	3.6	mA
t_{RST}	RST pulse width		200	500	1000	ns
V_{ad}	Auto-Detect threshold	Gate drive on; ramp V_{OUTsns}; monitor RST until it pulses.	-10	12	20	mV

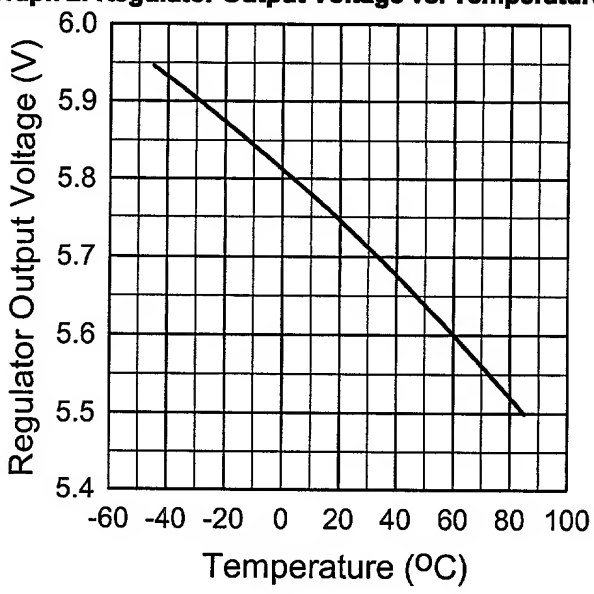
Note 1: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
Note2: All voltages are relative to ground unless otherwise specified.

Typical Performance Characteristics

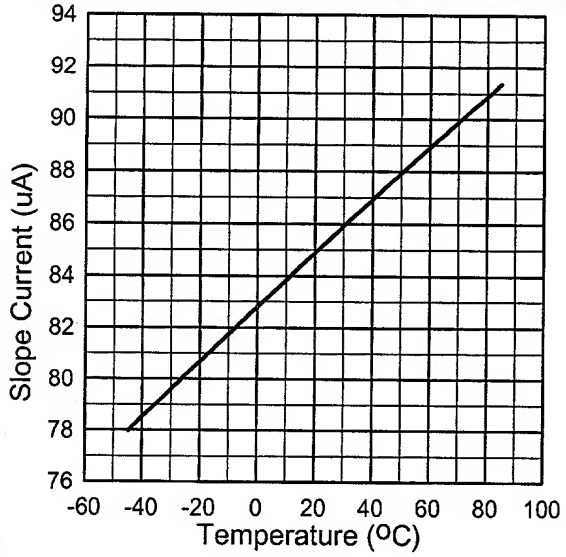
Graph 1: Icc vs. Temperature



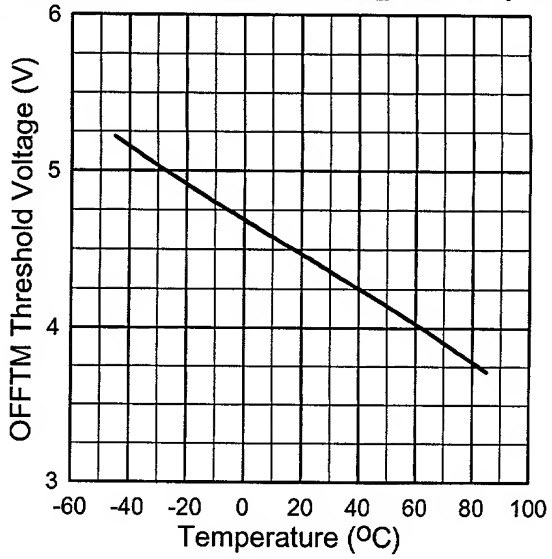
Graph 2: Regulator Output Voltage vs. Temperature



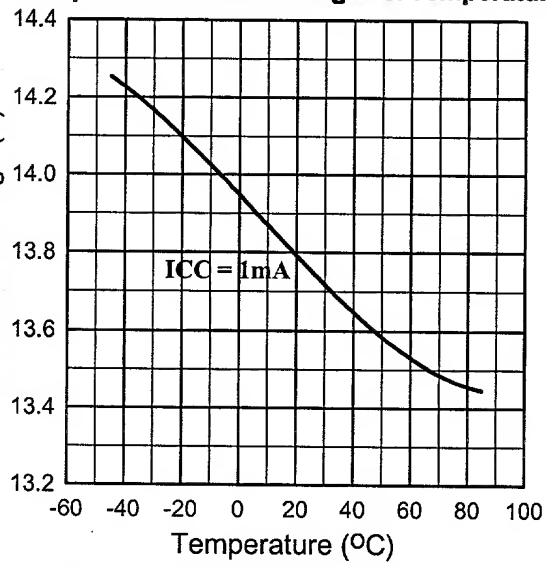
Graph 3: SLOPE Pin current vs. Temperature



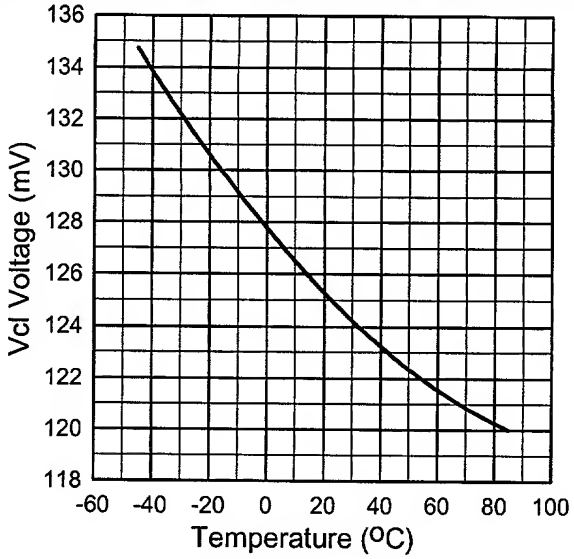
Graph 4: OFFTM Threshold Voltage vs. Temperature



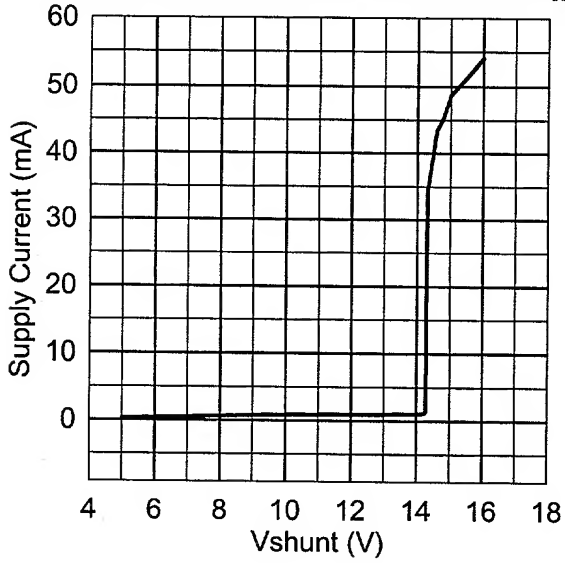
Graph 5: Vcc Shunt Voltage vs. Temperature



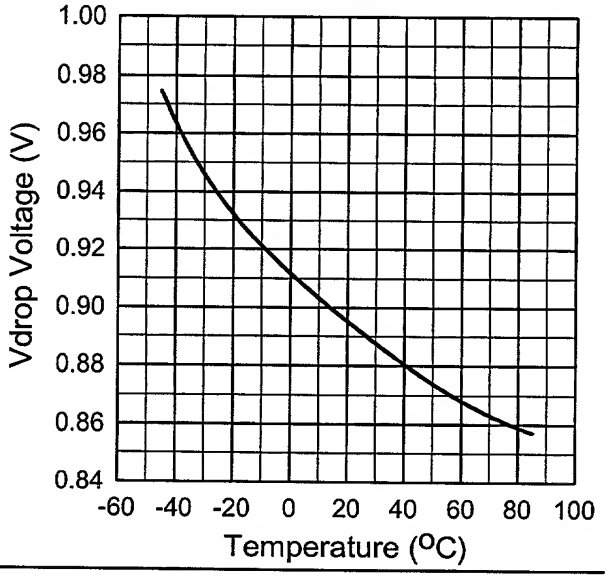
Graph 6: Overcurrent Threshold Voltage vs. Temperature



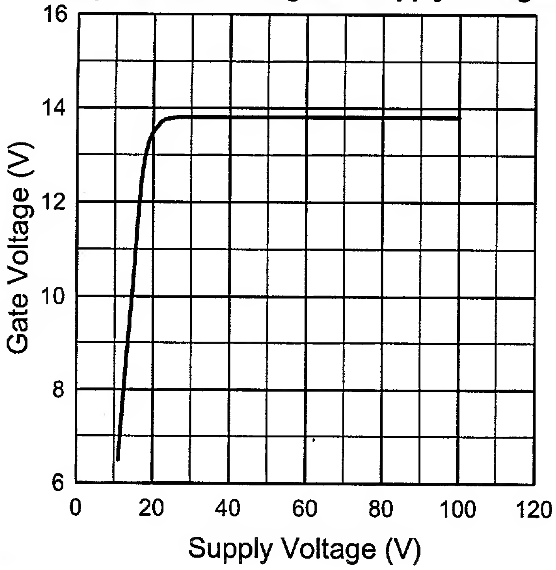
Graph 7: Supply Current vs. Shunt Voltage



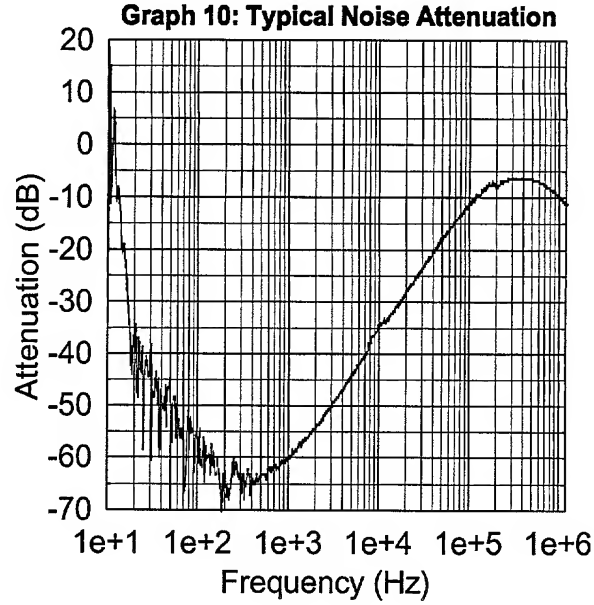
Graph 8: Vdrop Voltage vs. Temperature



Graph 9: Gate Voltage vs. Supply Voltage



Graph 10: Typical Noise Attenuation



Pin Descriptions

PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	INV	Invert Input	The invert input controls GSNSin's polarity. When invert input is high compared to AGND, then GSNSin low indicates an insertion/removal event. When invert input is low, then GSNSin high indicates an insertion/removal event.
15	GSNSin	Ground Sense Input	The INV pin controls the polarity sense of this input. A 3uA internal pull-up current source causes logic high when there is no connection at this pin. With INV low or connected to AGND, a GSNSin low (or connected to AGND) will keep RSTout and GATE low, and the external power switch, Q1, off. A disconnected GSNSin pin or when Vcc is applied to it will allow normal operation
2	VCCin	Supply Voltage	Positive power-supply voltage input.
3	SHNToff	Shunt Off	This pin serves to control the enabling of the shunt circuit. When the pin is high compared to AGND, then the shunt regulator is in off position. A low level at this pin activates the shunt regulator.
4	CAPin	Active low-pass filter capacitor input	The output of the power active filter tracks this pin. Adding an external RC network matching the input noise with respect to the 3db point of the filter could reduce the noise to a minimum.
5	VDROP	Active filter offset voltage	This pin sets the drop out MOSFET voltage across the active filter.
6	SLOPE	Slope input	This input controls the current slope during power up and controls inrush currents. Adding external capacitors to this pin allow regulation and adjustment of the rate of the current slope.
7	OFFTM	Off-time	The OFFTM pin sets the delay time between power-down and restart of IXHQ100. Delay time can be increased by adding external capacitors to this pin.
8	AGND	Ground	The IXHQ100 system zero reference pin.

Pin Descriptions (continued)

PIN #	SYMBOL	FUNCTION	DESCRIPTION
9	VDDout	Regulator output voltage	Regulator output voltage provides current to drive the external circuits with respect to AGND.
10	VCL	Overcurrent threshold bias voltage	Sets the overcurrent threshold bias voltage.
11	SOURCE	Current input sensor	Input for sensing current through power device with respect to AGND.
12	GATE	Output	Control voltage for driving external MOSFET.
13	OUTsns	Out sensor signal	This signal senses the output voltage of the circuit.
14	RSTout	Output Reset	A low at this pin indicates detection of an insert/removal event or overcurrent detection.
16	NC	N/A	Not Connected

IXHQ100 Logic Diagram

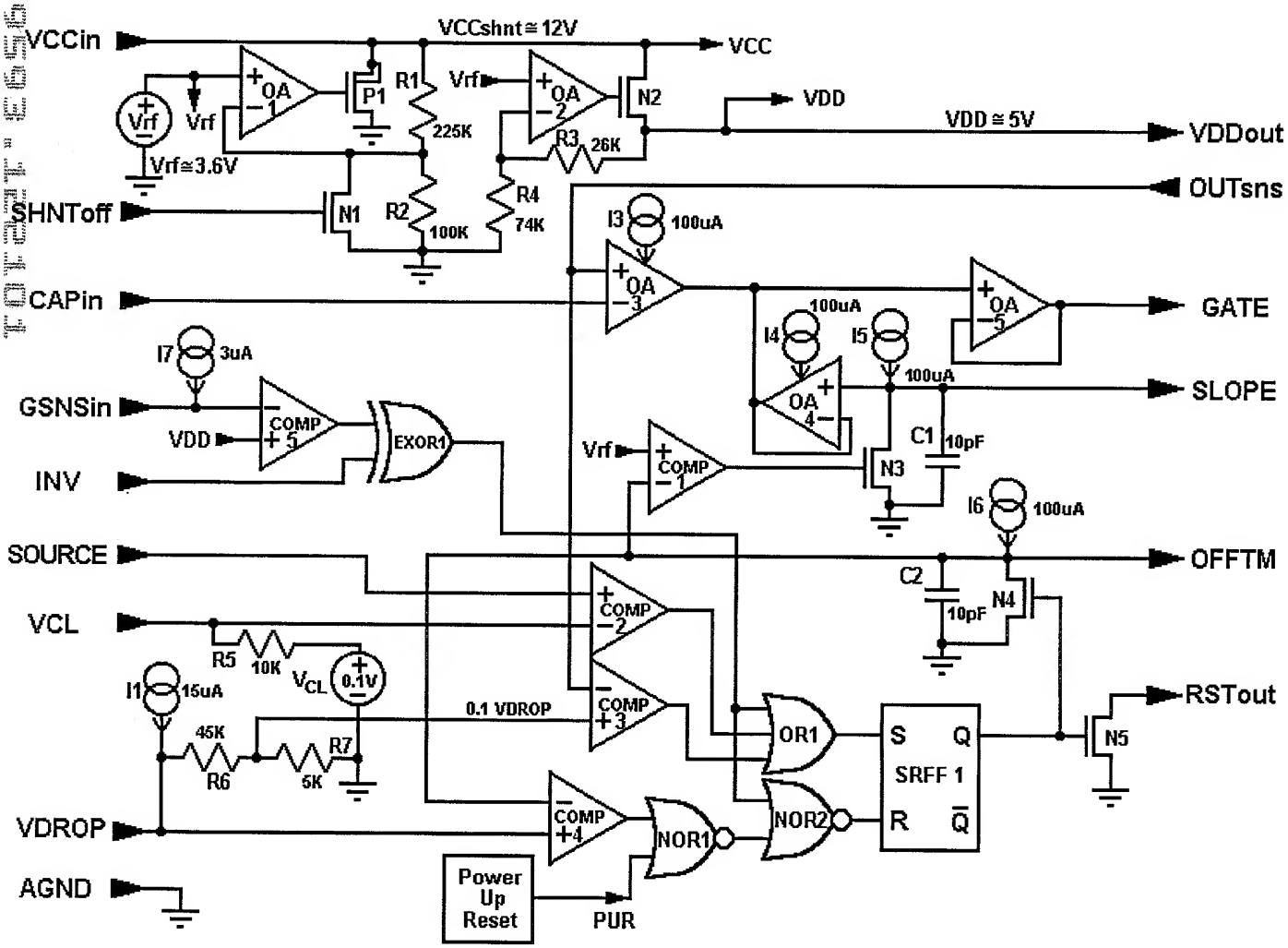


Figure 2

DEVICE OPERATION*

A hot swap operation involves removal and reinsertion of a device while the system using it remains in operation. Such an operation could cause external capacitors to draw currents high enough to disturb system operations or even cause permanent damage to both the device and the system.

The IXHQ100 is designed to prevent any disturbances or damage during such occurrences, allowing the circuit board to be safely inserted and removed from a live backplane. Capable of operating under three modes, the chip also acts as a power active noise filter and an auto-detect circuit.

Insertion Process

As the circuit board is inserted into the backplane, physical connections should be made to ground to discharge any electrostatic voltage. The insertion process begins when power and ground are supplied to the board through pins on the blackplane.

Once power is applied, the IXHQ100 starts up but does not immediately apply power to the output load. The internal Power Up Reset logic (see in Figure 2) turns on for 10 µs prior to any other logic. This pulse goes through two NOR gates and resets SRFF1 Flip Flop. Once SRFF1 is reset, the current source, I6, charges the OFFTM pin at a rate proportional to the size of the external capacitor, C7 (fig 1). During the time the OFFTM pin is ramping from 0V to Vrf (~5V), which is the $T_{off\text{-}delay}$, COMP1 keeps N3 ON so V_{SLOPE} stays at 0V. After $T_{off\text{-}delay}$, V_{OFFTM} becomes greater than Vrf, and COMP1 goes low, driving N3 to off state. I5 now starts to charge C1, ramping +ve i/p of OA4. OA4 buffers V_{SLOPE} and sets the GATE output ramp.

It is assumed that when the circuit board is first inserted into the backplane, the voltage across the external load, V_{load}, is zero. As V_{SLOPE} rises, its rate of increase determined by the value of the external capacitor, C8 (figure1), and the value of the internal current source, I5. V_{GATE}'s rate of increase follows V_{SLOPE}. As soon as V_{GATE} exceeds V_{thQ1} (figure 1) of the external power MOSFET, drain current I_{dQ1} starts to flow. The rate of increase of I_{dQ1} is proportional to the rate of increase of V_{SLOPE}, and is independent of the size of C5 , the total filter capacitance of the load. Note that this rate, which is directly proportional to C7 and inversely proportional to C8, could be adjusted . Similarly the Toff-delay can be adjusted and is directly proportional to the size of C7.

Normal Operation

With continuous $-V_{in}$ applied, the IXHQ100 acts as an active power filter by modulating the voltage drop across the external Power MOSFET V_{ds} so that any noise on $-V_{in}$ is cancelled by V_{ds}.

The direct connection of IXHQ 100's AGND pin to $-V_{in}$ allows the V_{drop} (internally set to ~750mV) to set the ~90% of the maximum peak noise voltage reject by the IXHQ100. The internal V_{drop} setting of ~750 mV allows 1.35 Vpp of noise rejection. Graph on page 5 illustrates the level of ripple attenuation during normal conditions. Notice that the noise rejection is very high (~60db) between 400Hz to 40KHz, which is optimal for most hot swap applications.

Flip-flop setting and resetting

The flip-flop, SRFF1 (fig 2), used in the IXHQ100, is reset dominant. Hence when both S and R inputs are driven high, the SRFF1 remains reset. Under normal operation, S input becomes high whenever OR1 output is high and R input is low. In turn, OR1 goes high if any one of the outputs of EXOR1, or COMP2, or COMP3 goes high.

EXOR1 output goes high if it detects the loss of either Gnd or -Vin. If INV input is connected to

*Unless otherwise stated, all symbol and device references are referred to the logic diagram (Fig 2) on page 6

Vcc, then GSNSin pin can be used to detect the presence or absence of -Vin. If INV is connected to AGND, then GSNSin pin can be used to detect the presence or absence of Gnd.

COMP2 output goes high whenever an overcurrent or a short circuit condition is detected. The inverting input to COMP2 is connected to the VCL output pin which is internally set at approximately 120mV. As shown in Figure 1, one side of R4 is in series with the source of Q1, the drain output of which drives the load connected to J8. The return side of R4 is connected to -Vin through J1. For R4 = 0.02Ω, Q1 source currents greater than 6A will turn on COMP2 and will be considered either an overcurrent or short circuit event.

COMP3 goes high whenever the voltage at OUTsns with respect to AGND becomes less than 0.1*VCL(approximately 12mV). This can only occur if either the current drawn by the driven load is less than 600mA (12mV/.02) or $-V_{IN}$ is disconnected. This Auto-Disconnect technique automatically detects load disconnections without needing additional sensors.

Thus the SRFF1 will reset when one of the following events occur:

1. Loss of AGND or -Vin.
2. Overcurrent or short circuit.
3. Auto-Disconnection

A valid S input into SRFF1 will immediately drive its output, Q1, to high and will turn on both N5 and N4. N5, an open drain output, will result in RSTout being driven low. A current limiting resistor, R1, in series with a 4N35 LED connected to V_{DD} (fig 1) can be used to generate an isolated reset pulse. Turning on N4 will discharge C7 and the internal 10pF capacitor (fig 2). As soon as V_{OFFTM} drops below V_{DROP} =~0.9V, COMP4 in Figure 2 will turn on through NOR1 and NOR2, and resets SRFF1 with a high applied to its R input. This act will then turn off both N5 and N4 and allow OFFTM pin to initiate its positive ramp as a result of I6 charging the capacitors C7 (Figure 1) and C2 (Figure 2) connected to the OFFTM pin.

Restart Operation

The IXHQ100 will automatically attempt to restart once a disconnection and reconnection is detected. Either PUR or COMP4 going high will reset SRFF1 during normal operation of the IXHQ100 (fig 2). Resetting SRFF1 turns off N4 and N5, and the OFFTM pin ramps up in response. During this ramp, as long as V_{OFFTM} is less than Vrf=~4.5V, COMP1 will keep N3 on and C1 (Figure 2) and C8 (Figure 1) discharged. After $T_{off\text{-}delay}$, V_{OFFTM} is at Vrf, COMP1 output then goes low, turning off N3. Now the SLOPE pin is free to ramp up as a result of I5 charging C1 (Figure 2) and C8 (Figure 1). The two unity-gain buffers, OA4 and OA5, reflect V_{SLOPE} at the GATE output pin during this positive ramp. As soon as V_{GATE} overcomes the V_{Q1th}, normal operation is resumed.

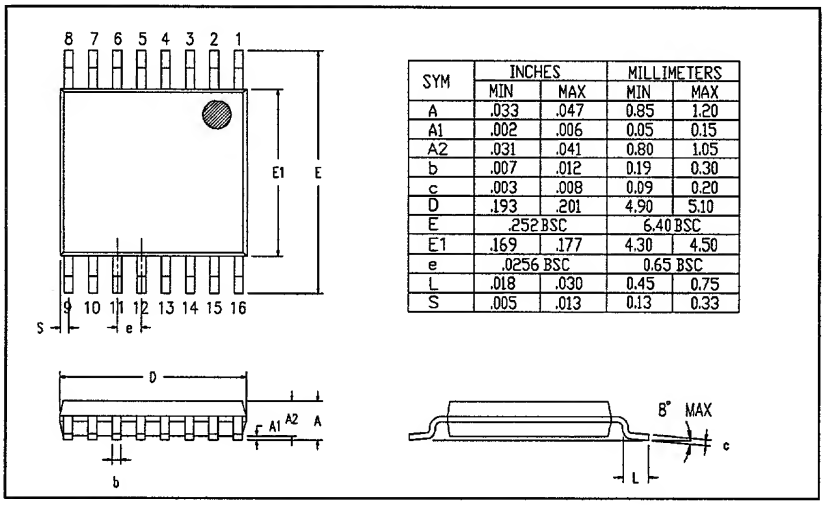
Fault Operation

When the output load current is such that the voltage drop across the current sense resistor between the SOURCE pin and the AGND exceeds VCL (internally set to ~120 mv), the GATE output is driven low to turn off the external Power MOSFET connected between the load and $-V_{in}$. An external capacitor connected between OFFTM pin and AGND pin determines the off time $T_{off\text{-}delay}$. IXHQ100 will restart the turn on sequence of the external Power MOSFET with a load voltage slope determined by the size of the external capacitor that is connected to the SLOPE pin.

Short Circuit Prevention

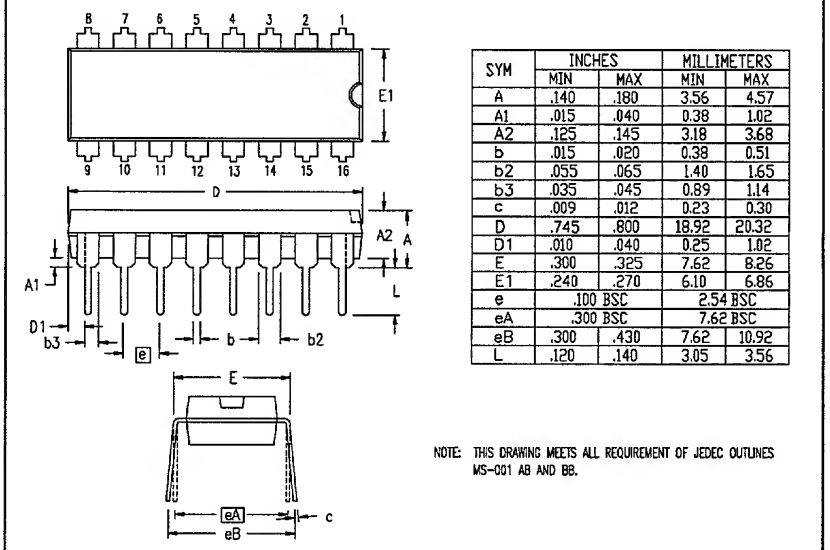
When the IXHQ100 detects a short in the load, a restart is automatically initiated. The GOUT drops to zero and waits one $T_{off\text{-}delay}$ before SLOPE ramps up. As before, normal operation is resumed.

Package Outlines: 16 PIN TSSOP



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.033	.047	0.85	1.20
A1	.002	.006	0.05	0.15
A2	.031	.041	0.80	1.05
b	.007	.012	0.19	0.30
c	.003	.008	0.09	0.20
D	.193	.201	4.90	5.10
E	.252 BSC		6.40 BSC	
E1	.169	.177	4.30	4.50
e	.0256 BSC		0.65 BSC	
L	.018	.030	0.45	0.75
S	.005	.013	0.13	0.33

Package Outlines: 16 PIN PDIP



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.745	.800	18.92	20.32
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 AB AND BB.

Ordering Information

Part Number	Package Type	Grade
IXHQ 100PI	16 PIN PDIP	Industrial
IXHQ 100SI	16 PIN TSSOP	Industrial

IXYS Corporation
3054 Bassett St; Santa Clara, CA 95054
Tel: 408-982-0700; Fax: 408-496-0670
e-mail: sales@ixys.com

IXYS Semiconducotr GmbH
Edisonstrasse15 ; D-68623; Lampertheim
Tel: +49-6206-503-0; Fax: +49-6206-503627
e-mail: marcom@ixys.de